



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,289	12/28/2001	Young-Hun Ha	8733.560.00	2930

30827 7590 02/11/2005

MCKENNA LONG & ALDRIDGE LLP  
1900 K STREET, NW  
WASHINGTON, DC 20006

EXAMINER
----------

DI GRAZIO, JEANNE A

ART UNIT	PAPER NUMBER
----------	--------------

2871

DATE MAILED: 02/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/028,289

Applicant(s)

HA ET AL.

Examiner

Jeanne A. Di Grazio

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on Amendment of 10 Nov. 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 9 and 12-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10, 11, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2871

## **DETAILED ACTION**

### ***Claims***

Claims 1-8, 10-11, 21 and 22 are pending with claims 1, 2, 4, 7 and 10 having been amended per Amendment of November 10, 2004. New claims 21 and 22 are added per Amendment of November 10, 2004. Claims 9 and 12-20 have been previously withdrawn per Applicant's election with traverse of Species A (claims 1-8 and 10-11 readable thereon) in the reply filed on May 21, 2004.

### ***Priority***

Priority to Korean Patent Application No. 2000-85421 (Dec. 29, 2000) is claimed.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,204,907 B1 (to Hiraishi et al.)(filed: Aug. 27, 1996).

Art Unit: 2871

As to claim 1 (amended), Hiraishi discloses, with reference to Figure 3, a lower substrate (11) including a seal pattern forming region between a display area and a non-display area of the lower substrate (11) wherein an interlayer insulating film (9) (Applicant's "passivation layer") is removed in the periphery of the display (Applicant's "wherein a passivation layer is removed in the non-display region")(See also Column 10, Lines 51-55)(stating "[a] periphery of the display area, i.e., a part of the interlayer insulating film under a portion where the seal is provided is removed during the patterning of the interlayer insulating film in the same manner as the contact hole portion is removed."), a gate insulating layer (5) on the lower substrate (11) in the display area and the non-display area of the lower substrate (the gate insulating film (5) extends into both peripheral and display regions), an upper substrate (20), a seal pattern of a constant thickness (14) formed on the gate insulating layer (5) in a boundary between the display area and the non-display area of the lower substrate (11) and a liquid crystal layer (8) between the upper substrate (20) and the lower substrate (11).

As to claim 2 (amended), Hiraishi features the lower substrate (11) as having an insulative substrate (this is the TFT substrate). The insulative substrate extending across the display area and the non-display area.

As to claim 3, the lower substrate (11) further includes gate wirings (1), a gate insulation film (5), a thin film transistor substrate (collectively 10), source wirings (2) and ITO therein (Column 10, Lines 26-35) and pixel electrodes (4).

As to claim 4 (amended), the upper substrate includes a color filter substrate and opposite electrodes (6).

As to claim 6, Hiraishi further has spacers (7 and 13).

Art Unit: 2871

As to claim 10 (amended), Hiraishi discloses, with reference to Figure 3, a lower substrate (11) having a display area and a non-display area of the lower substrate (11) an interlayer insulating film (9) (Applicant's "passivation layer") is removed in the periphery of the display (Applicant's "wherein a passivation layer is removed in the boundary region") (See also Column 10, Lines 51-55) (stating "[a] periphery of the display area, i.e., a part of the interlayer insulating film under a portion where the seal is provided is removed during the patterning of the interlayer insulating film in the same manner as the contact hole portion is removed."), a gate insulating layer formed (5) on the lower substrate (11) in the display area and the non-display area (the gate insulating film (5) extends into both peripheral and display regions), an upper substrate (20) having an area corresponding to the display area and the non-display area, the upper substrate (20) and the lower substrate (11) spaced apart and facing each other, a seal pattern of a constant thickness (14) formed between the upper substrate (20) and the lower substrate (11) along a boundary region between the display area and the non-display area.

Hiraishi explains that the liquid crystal can be thus smoothly injected (Column 10, Lines 39-40 and entire patent) and thus it may be inferred that the seal (14) must have an injection hole and that the liquid crystal is injected through the injection hole. It may thus also be inferred that once the liquid crystal is injected through the injection hole, the injection hole must then be sealed off to prevent liquid crystal matter from escaping through the injection hole. Please also note that the seal (14) contacts the gate insulating film (5).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of United States Patent 6,336,331 B1 (to Sakamoto et al.).

As to claim 5, Hiraishi does not appear to explicitly specify that the passivation layer is removed during a photolithographic mask step for simultaneous patterning of an active layer and the passivation layer.

Sakamoto teaches and discloses an active matrix liquid crystal display device having improved terminal connections in which an organic film and passivation film are patterned simultaneously (Column 3, Lines 50-55). Such simultaneous patterning results in a good contact

Art Unit: 2871

between a terminal and a TAB in an active matrix substrate (Id.) and results in improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Sakamoto is evidence that ordinary workers in the field of liquid crystal would have found the reason, suggestion, and motivation to simultaneously pattern an organic film and passivation film for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystal at the time the invention was made to modify Hiraishi in view of Sakamoto for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.).

As to claims 7 (amended) and 8, Applicant's recited method steps of fabricating a liquid crystal panel for liquid crystal display devices would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in view of the device as recited and taught by Hiraishi.

Art Unit: 2871

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of Japanese Patent Application 02-220032 (to Obara et al.).

As to claim 11, Hiraishi does not appear to explicitly specify that the seal pattern is formed by a screen-printing process using thermosetting resin that includes glass fiber.

Obara teaches and discloses an electro-optic device wherein a thermosetting epoxy resin is used as a seal, the thermosetting epoxy resin is made by screen-printing and contains glass fiber spacers for seal strength and uniformity (Abstracts).

Obara is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to form a thermosetting seal with glass fibers by screen printing for seal strength and uniformity.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Hiraishi in view of Obara for seal strength and uniformity.

Claims 21 and 22 (both new) are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,204,907 B1 (to Hiraishi et al.) in view of United States Patent 5,909,263 (to Song).

As to claims 21 and 22, Hiraishi does not appear to explicitly specify that the passivation layer is removed in each of a plurality of pixel regions.



Art Unit: 2871

Song teaches and discloses a liquid crystal display panel array structure at a pixel contact hole (entire patent) and teaches that a portion of a passivation layer is removed in a pixel region in order to form a pixel contact hole (Column 2, Lines 43-52).

Song is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to remove a portion of a passivation layer in a pixel region so that necessary contact holes could be formed.

Therefore it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Hiraishi in view of Song for the formation of necessary contact holes.

#### ***Response to Arguments***

Applicant's arguments with respect to claims 1, 7 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2871

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2871

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289.

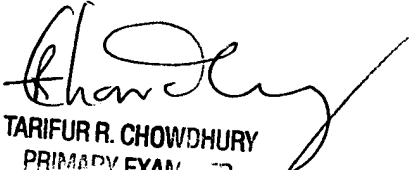
The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio  
Patent Examiner  
Art Unit 2871

JDG

  
TARIFUR R. CHOWDHURY  
PRIMARY EXAM